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Design and Performance analysis of Low power CMOS Op-Amp

Anand Kumar Singh[*1], Anuradha[2], Dr. Vijay Nath[3]

[*1,2] Department of Electronics and Communication Engineering, Ajay Kumar Garg Engg. College, Ghaziabad, India

[3]BIT Mesra Ranchi, Jharkhand

anand321elex@yahoo.com

Abstract

This paper proposes a low power CMOS operational amplifier which operates at 1.8 V power supply. The unique behavior of the MOS transistors in sub-threshold region not only allows a designer to work at low input bias current but also at low voltage. While operating the device at weak inversion results low power dissipation but dynamic range is degraded. Designing of two-stage Op-Amp is a multi-dimensional optimization problem where optimization of one or more parameters may easily result into degradation of others. The Op-Amp is designed to exhibit a unity gain frequency of 17.3 MHz and exhibits a gain of 62.04dB. The proposed design uses a smaller compensation capacitor (CC), which improves the slew rate and also, benefits for the area of compensation circuit. In order to verify the viability two-stage Op-Amp at SCNO 180 nm CMOS technology is designed and verified and power consumption is reduced.

Keywords: Low power CMOS Op-Amp, gain bandwidth product, gain margin, phase margin

Introduction

CMOS Op-Amps are ubiquitous integral parts in various analog and mixed-signal circuits. The term OTA was originally conceived for operational transconductance amplifiers with linear transconductance (used for the implementation of continuous-time filters), for the sake of simplicity we will use the same term OTA for general operational trans conductance amplifiers. The two-stage Op-Amp shown in Fig. 1 is widely used because of its simple structure and robustness. The method handles a very wide variety of specifications and constraints, is extremely fast, and results in globally optimal designs [1]. In designing an Op-Amp, numerous electrical characteristics, e.g., gain-bandwidth, phase margin common-mode range, offset, all have to be taken into consideration [2]. Furthermore, since Op-Amps are designed to be operated with negative-feedback connection, frequency compensation is necessary for closed-loop stability [3]. Unfortunately, in order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised [4]. As a result, designing an Op-Amp that meets all specifications needs a good compensation strategy and design methodology. Designing high-performance analog integrated circuits is becoming increasingly exigent with the flexible trend toward reduced supply voltages [5]. Speed and accuracy are two most important properties of analog circuits, however optimizing circuits for both aspects leads to contradictory demands. At large supply voltages, there is a tradeoff among various performance parameters. The realization of a CMOS Op-Amp that combines a considerable dc gain with high unity gain frequency has been a difficult problem. There have been several circuit approaches to evade this problem. The simulation results have been obtained and verified using 180nm SCNO MOSIS Design and carried out in Cadence virtuoso.

Proposed Method

The basic equations and parameters are described below. These design main parameters are: phase margin (M_Φ), gain-bandwidth product (f_{GBW}), load capacitance (C_L), slew rate (SR), input common mode range ($ICMR$),In this circuit replacing the current source and uses PMOS active load. Using formula in current and resister and accepted ratio

$$R = 1/K'S(V_{GS}-V_T) \quad (1)$$

Where $S=W/L$ and $K'=\mu_0 C_{OX}$

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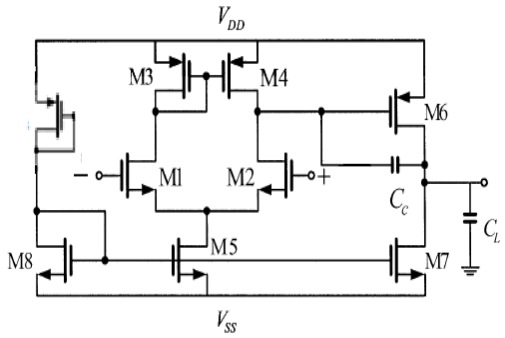

Fig. 1 Two stage Op-Amp

The equations for determining the various Op-Amp characteristics can be shown as follows:

Gain and Bandwidth

The dc gain of Op-Amp is given by

$$A=20 \log V0/VIN \quad (2)$$

By placing differential pair M1, M2, M3,M4. It is possible to obtain rail to rail input stage.

Common Mode range

If we define V_{CM} as the Op-Amp input common mode range i.e

$V_{CM}^{+} = V_{DD} - V_{CM}(max)$ (3)

and $V_{CM}^{-} = V_{CM}(min) - V_{SS}$ (4)

Internal Slew Rate

The slew rate associated with C_C is found to be

$$SR = \frac{I_{D5}}{C_C} \quad (5)$$

1.2 External Slew Rate

The slew rate associated with C_L is found to be

$$SR = \frac{I_{D7} - I_{D5}}{C_L} \quad (6)$$

Combining both above equations we obtain

$$I_{D7} = SR(C_C + C_L) \quad (7)$$

Design Steps for Two-Stage OP-AMP

In this work, an Op-Amp has been designed which exhibits high unity gain frequency for optimized balancing of phase margin, gain, power and load. A method is proposed to set a higher unity gain frequency of the Op-Amp working at a lower supply voltage. This allows the value of each circuit element of the amplifier (i.e. transistor aspect ratios, bias current and compensation capacitor) to be univocally related to the required electrical parameters [6] & [7]. Here we have chosen a simple differential pair amplifier for input amplifier, common source amplifier (high gain, swing balancing) for output amplifier, a current mirror circuit and a biasing circuit, and connecting PMOS load in input (replacing current source) with a Miller capacitance in series with each other. We see that simulate in above circuit and get DC Gain 54db and GBW 18.15 MH_Z. Then we connected same W/L ratio in series PMOS and NMOS IN Load. A design steps for two-stage Op-Amp in Figure 2 can be constructed as follows.

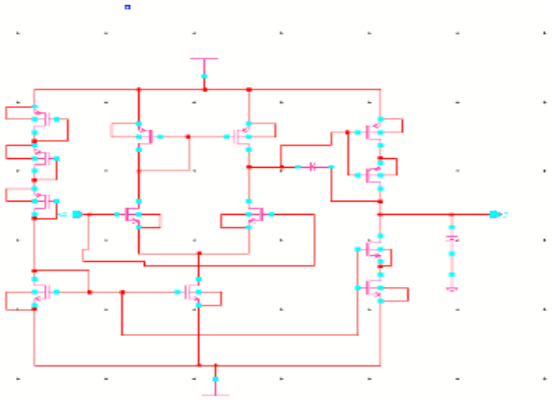

Fig. 2 The proposed CMOS Op-Amp circuit

A design steps for two-stage Op-Amp in Figure 2 can be constructed as follows.

STEP-1 The equation of S_1 and S_2 is

$$S_1 = S2 = (W/L)_1 = \frac{g_{m1}}{K1I5} \quad (8)$$

$g_{m1} = GB*Cc$ & $Cc = 0.2\ C_L$

STEP-2 The equation of Vss_5 is

$$V_{ss5(SAT)} = V_{in(min)} - Vss - \sqrt{I_5/\beta 1} - V_{T1} \quad (9)$$

STEP-3 The equation of S_3 is

$$S_3=2I_3/K_3[V_{DD}-V_{in(max)}-V_{T(max)}+ V_{T(min)}]^2 = S_4 \quad (10)$$

STEP-4 The equation of S_5 is

$$S_5= 2\ I_5/K_3[V_{DSS5(sat)}]^2 \quad (11)$$

STEP-5 The equation of S_6

$$S_6 = (g_{m6}/g_{m4})S_4 \quad (12)$$

STEP-6 The equation of I_6

$$I_6 = gm_6/2\ K_6S_6 \quad (13)$$

STEP-7 The equation of S_7 is

$$S_7 = (I_6/I_5)S_5 \quad (14)$$

$$S_9= S_{10}= S_{11}=\frac{1}{KR(Vgs-VT)} \quad (15)$$

Simulation Results

Based on the proposed circuit in Figure 2 Op-Amp has been designed 180nm CMOS technology. The Op-Amp is currently being fabricated in SCNO so only the post simulation results will be presented here. Fig.3 presents the simulated results of for V_{dd}=1.8V. The process parameter and the electrical specification of CMOS Op-Amp for 180 nm CMOS technology are tabulated in the Table I and Table II respectively.

Table i

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Electrical specification of cmos op-amp

Load capacitance: C_L (pF)	10
Miller compensation capacitances: C_C (pF)	3
Supply voltage	+1.8 V

Table ii
Process parameters (scno180 nm tech.)

$\mu C_{ox}/2$: NMOS (A/V²)	173.9
$\mu C_{ox}/2$: PMOS (A/V²)	35.0
V_{thpmin} (volt)	0.37
V_{thnmax}(volt) NMOS	0.50
ICMR(Volt)	1.3
Vdd(volt)	1.8

Table iii
Device size for two stage op-amp

Device size S=W/L	Unit nm
S1	4500
S2	4500
S3	1260
S4	1260
S5	1620
S6=S6A	17820
S7=S7A	15300
S8	1620
S9	540
S10	540
S11	540

AC Response

Through AC response we can simulate the schematic to find out the bode plot and phase plot. In Figure 3.1, a bode plot and phase plot for 1.8 V, 27° C and C_L = 10 pf is shown. As it can be seen, the open loop gain is 62.05 dB, and a phase margin is 166.3°. The unity gain bandwidth is 17.15MHz bandwidth is 1.74 KHz

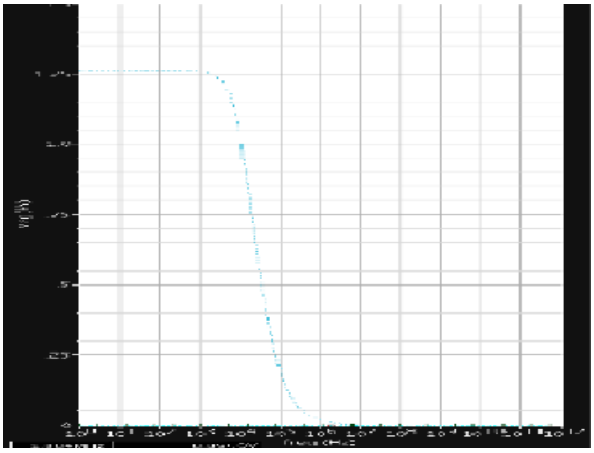

Fig. 3.1 Frequency Response Plot with C_L=10 pf

Transient Step Response

In Figure 3.2, a step from ground to V_{DD} is applied at the input with unity feedback configuration and slew rate of 11.22 V/µS for rising edge of pulse and 11.10 V/ µS for falling edge of the pulse is obtained.

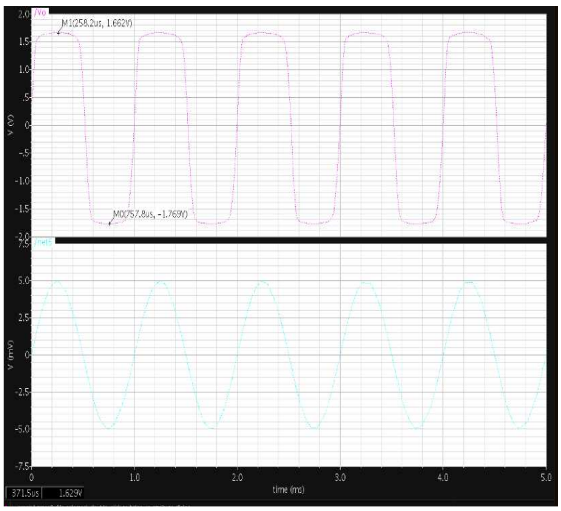

Fig. 3.2 Transient Pulse Response of Op-Amp

Gain and phase

Fig 3.3 and Fig3.4 show DC gain and phase of Op-Amp at SCNO 180nm technology. The obtained DC gain is 62dB and phase 179 degree at V_{dd}=1.8V.

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Fig. 3.3 DC Gain of Op-Amp

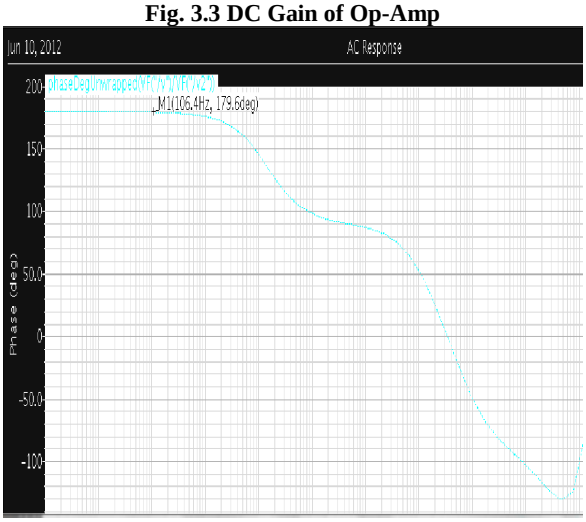

Fig.3.4 Phase of Op-Amp

Phase Margin and Gain Margin

Figure 3.5 shows that the obtained phase margin 13.69degree and gain margin is 28.36dB after simulation with applied voltage of 1.8V and gain of 62dB and phase of 179degree.

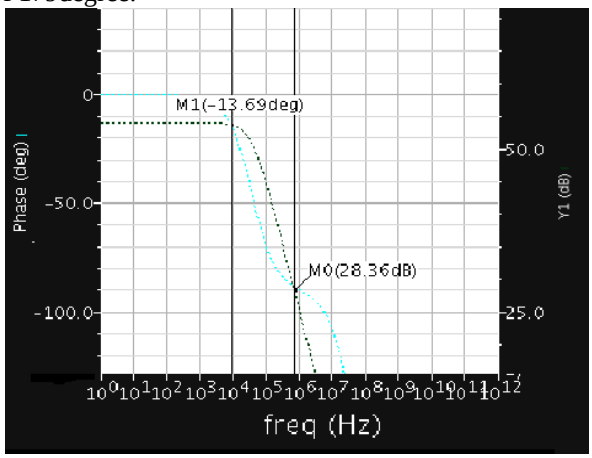

Fig. 3.5 .phase and gain margin of Op-Amp

Table IV
Simulation Results for Op-Amp (180nm Technology)

Specifications	Theoretically value	Simulation results
DC gain (dB)	54	62.05
GB (MHz)	17.3	18.9
Phase margin	155.2	166.31
ICMR (V)	1.3	1.0
Slew rate (V/μS)	10.8	11.23
I_{D5}(μA)	32.4	33.78
I_L(μA)	140.4	141.8
Load capacitance (pf)	10	10
Supply voltage (V)	1.8	1.8

Conclusion

The proposed Op-Amp is simulated at 180 nm using cadence virtuous and performance is measured as table IV. The excellent results of dc gain and Slew rate are obtained by the proposed structure. The dc gain and GBW graphs show increase DC gain decrease GBW frequency also bandwidth of Op-Amp is increased to balance DC Gain being a good characteristic amplifier. If frequency increases then this amplifier can work as oscillator so we have to balance condition in both. Design technique for this Op-Amp, its calculations and computer-aided simulation results are given in detail. The results show that the designed amplifier has successfully satisfied all the specifications given in advance. Tables and graphs of different parameters for various aspect ratios are drawn. As a summary, tables and graphs are provided to estimates the scaling limits for various applications and device types. The end result is that there is no single end point for scaling, but that instead there are many end points, each optimally adapted to its particular applications to determine the dc gain improvement.

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